In the Specification:

Please amend the specification as follows:

Change paragraph 0002 change to:

[0002] Typical semiconductor devices comprise multiple circuits formed within a dielectric region comprised of one or more dielectric layers on top of a silicon substrate or wafer. On top of the substrate are layers of dielectric and layers of metal and layers of metal embedded in dielectric. When the metal interconnect leads of the circuits are on different layers, conductive vias extend through the dielectric layers to make connections between the wiring leads on different interconnect levels. Sometimes, based on the circuit design, a significantly large amount of current may flow through the metal interconnect leads, causing Joule heating to increase the temperature of the metal leads. The current flowing through these leads may cause sufficient Joule heating to increase the temperature of the leads. Such temperature increases may accelerate reliability wearout mechanisms such as ~~eletromigration~~ electromigration and stress migration that might possibly lead to failure of the integrated circuit. It is common practice to widen leads that have current densities in excess~~ive~~ of those required for reliable operation. However, widening leads may have a deleterious impact on the area of the integrated circuit.

Change paragraph 0012 to

[0012] Figure 7 illustrates a perspective view of the case where the mechanical cooling fin or inactive conductive conductor is in the shape of an "H" and is in the same heat dissipating layer as the via ~~In~~ in Fig. 2 and Fig. 3 for a single damascene process.

Change paragraph 0016 to:

[0016] Figures 1-3 shows one embodiment of the present invention for reducing the temperature rise due to Joule heating. Figure 1 is a top plan view of the integrated circuit 10 according to embodiments of the present invention described in connection with Fig. 2-7. Figure 2 is a cross section taken though A-A in Figure 1 and Figure 3 is an orthogonal cross section taken through B-B in Figure 1. The integrated circuit 10 includes an integrated circuit substrate 24 of silicon, for example, having a top surface 26 and bottom surface 28 and dielectric body ~~region or layer~~ 18 above the substrate 24 with a bottom surface 22 adjacent with the top surface 26 of the substrate 24. The dielectric body ~~region or layer~~ 18 may include silicon dioxide, silicon nitride, or other suitable dielectric material. The dielectric body ~~region or layer~~ 18 comprises multiple layers of heat generating leads or other structures embedded within the dielectric body ~~region~~ 18, such as an electrically active current carrying metal lead 13 in layer 18a. The metal lead 13 is represented by dashed lines in Figure 1 since the lead 13 is in a layer 18a below the top surface of the dielectric body. The heat generating electrically active current carrying metal lead may include copper, aluminum tungsten, or other suitable metal or metal alloy. The dielectric ~~region~~ body 18 has at least one of its two surfaces – top and bottom – thermally coupled to an external heat sink by virtue of its packaging details. The heat dissipating surface can be either a bottom silicon substrate connected by bonding to a package or a top surface of an integrated circuit package. For simplicity, we will refer to the case where heat flow is through the bottom surface 22 connection to the integrated circuit substrate 24 at the top surface 26, although it is understood that the invention applies to the case where the other or both surfaces are thermally coupled to heat sinks.

There should be external ~~heart~~ heat sinks, as part of the details of integrated circuit packaging and the mounting of packages in the systems.

Change paragraph 0017 to:

[0017] In accordance with one embodiment of the present invention thermal cooling conductor or fin 14 is located in a substantially horizontal region or layer 17a in the dielectric ~~region~~ body 18 below an interconnect connector 13 layer 18a. This cooling fin is represented by dashed lines in Figure 1 since this is also below the top surface. The cooling fin 14 is physically connected to the electrically active interconnect conductor 13 to help dissipate the heat generated in the electrically active interconnect conductor 13. This cooling fin 14 in layer 17a provides an enhanced heat dissipating layer. The thermal cooling conductor or fin14 includes electrically inactive metal conductor such as a straight heat conductive line 14 physically connected by a connecting conductor via 15 extending in layer 18b between layers 18a and 17a of dielectric body 18 to the electrically active interconnect lead 13 in which Joule heating is being generated. Only a portion of the electrically active interconnect lead 13 is shown in the Figures 1-3.

Change paragraph 0020 to:

[0020] In the case where the dominant heat sink direction is above the dielectric ~~region~~ body 18 or for other reasons, the electrically inactive cooling fin 14 or enhanced dissipating layer would be in a layer of the dielectric body 18 above the electrically active interconnect line 13 and the placement of the elements in Fig. 1-3 would be reversed with fin 14 closer to the top of the dielectric ~~region~~ body 18 where the top heat sink is located in the place of active interconnect line 13 in Figures 2 and 3 and the location of the

interconnect line 13 would be below the fin 14 and in the place of fin 14 in ~~Figs.~~ Figures 2 and 3.

Change paragraph 0021 to:

[0021] In general, the electrically active interconnect lead can be connected to a cooling fin or electrically inactive line which is on ~~ant~~ one dielectric layer or level of the dielectric body 18 above or below the level of electrically active interconnect line to provide an enhanced heat dissipating layer or structure by the fin or electrically inactive line in the dielectric body. Whether it is above or below depends on whether the dominant heat sinking direction is above or below the dielectric ~~region~~ body 18, respectively. As an example, in the case where the dominant heat sinking direction is through the substrate 24, there may be multiple vias 15 between the electrically active interconnect lead 13 and the inactive cooling fin 14 as illustrated in Figures 4 and 5. Figures 4 and 5 are cross sections of Figure 1 taken at planes A-A for Figure 4 and plane B-B for Figure 5. The connection between the two vias 15 may include a conductive pad or block 17 at layer 18a. The closer the cooling fin 14 can be placed to the heat sinking substrate 24 for example the more optimal will be the temperature reduction of the electrically active lead. If on the other hand the heat sinking surface is at the top, the closer to the top the better.

Change paragraph 0024 to:

[0024] In accordance with another embodiment of the present invention, the electrically inactive heat dissipating cooling fin 14 is built in the same layer as the electrically active interconnect line 13 and is in fact a heat dissipating stub connection off the active line. The shape can be other than a straight line. ~~extending and fabricated~~

~~when the interconnect line is formed.~~ It can, in the most general embodiment, be any arbitrary shape which does not interfere nor come in contact with any other intentionally routed metal interconnect lines or substrate used to achieve circuit functionality. The fins have to be designed so as not to interfere with the other electrical lines, and in a manner that has acceptable parasitic capacitance.

Change paragraph 0025 as follows:

[0025] The presence of dummy metal structures increases the conductivity of heat to the substrate 11 and a heat sink. The electrically inactive cooling fin may be lines up with dummy metal structures 33 as illustrated in Figures 8, 9 and 10. In Figures 8 and 9 the electrically inactive cooling fin 14 extends along several dummy metal structures 33 below the cooling fin that aid in the conduction of the heat to the substrate ~~11~~ 24. In Figure 8 these dummy metal structures 33 are represented by dashed lines because they are below and aligned with the upper dummy metal structures 30 and the cooling fin 14. In Figure10 the electrically inactive cooling fin 14 is lined up with a dummy metal structure 33 that is located between the cooling fin and the substrate ~~11~~ 24.